

second substrate comprises an inner power core sandwiched between said pair of outer signal cores.

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b2
cont. } 14. (Added) The multi-layered circuit structure in accordance with claim 13, wherein said via through holes of said inner power core comprise undercut contact surfaces, and said via through holes of said spaced-apart outer signal cores each have metallic pads that make electrical contact with said undercut contact surfaces of said via through holes of said inner power core.

R E M A R K S

Reconsideration of the above-identified patent application is respectfully requested in view of the foregoing amendments and following remarks. Claims 2 through 4, 6, and 7 have been amended to reduce the ambiguities between "signal core" and "signal core layer", and "power core" and "power core layer", in accordance with 35 U.S.C. §112. New claims 11 through 14 have been added. Claims 8 through 10 have been canceled in accordance with the restriction requirement.

Claims 1 through 7, and 11 through 14 remain in this application.

The invention features a circuit board laminate comprising an inner power core that is connected between two signal cores. Upon lamination of the cores, the circuit board structure is electrically connected. The laminated circuit board inner power core comprises filled via through holes of conductive adhesive. The conductive power core vias make contact with the metal pads of the conductive vias of the respective outer signal cores, upon lamination. Claims 1 and 5 recite the structure defining the electrical connection between only one outer signal core and the inner power core. Claims 4, 7, and new claim 11 recite the complete sandwich structure comprising two spaced-apart outer signal cores laminated about a middle power core.

The rejection of claims 5 through 7 under 35 U.S.C. §102(b) as anticipated by SWAMY is respectfully traversed for the following reasons:

The patent to SWAMY teaches insulating layers 102 disposed between pairs of multilayered circuit sheets MLB #1,

2, 3, etc., of a circuit construction. The interconnecting sheets 102 comprise solder columns 106. The solder columns 106 run through the insulating layers to electrically connect the "blind vias" of the adjacent MLB sheets, as shown in FIGURE 2.

The illustrated structure of SWAMY is totally different from what is illustrated and claimed by Applicants in this application. SWAMY describes multilayered boards "MLB" that are separated by insulating layers. By contrast, Applicants claim a single (non-laminated) power core (layer) directly attached to a single (non-laminated) signal core (layer). There are no insulative sheets disposed between these two single sheets in Applicants' structure. The vias of Applicants' structure are not "blind" vias, but rather are shown and claimed as "through hole" vias (see FIGURE 3). In the dependent claims, the power core (single sheet) has "through hole" vias 16 that are filled with conductive adhesive. Other than being multilayered, the SWAMY laminated boards, designated MLB, are not power core or signal core elements. With all due respect, the Office has read Applicants' invention into the SWAMY reference.

The rejection of claims 1 through 3 and 5 through 7 under 35 U.S.C. §103(a) over SWAMY in view of BHATT et al is respectfully traversed for the following reasons:

SWAMY does not show the overall claimed structure of Applicants, as aforementioned. BHATT et al shows conductive material in the vias, but not for the purpose taught by Applicants. BHATT et al flows conductive material from the surface of the circuit board into the holes, as a means of connecting the circuit to the vias. Applicants, by contrast, teach electrically connecting a via of the signal core with the via of the power core. Not only is the purpose and structural teaching different, but the connection is made during lamination of the two cores, about which BHATT et al is totally silent. It is obvious to this attorney that the Office is applying BHATT et al to this invention in a hindsight manner.

The rejection of claim 4 under 35 U.S.C. §103(a) as unpatentable over SWAMY in view of BHATT et al, and further in view of CARR et al is traversed for the following reasons:

SWAMY does not show the claimed structure: BHATT et al does not have the same purpose and structure for his conductive vias; and CARR et al does not show conductive pads. Applicants' pads are flat, and make contact when the boards are laminated together. By contrast, CARR et al shows elevated lands, which are not used to connect the via of one layer with the via of an adjacent layer. CARR et al is neither structurally the same, nor does it teach the same structural purposes as Applicants' invention. With all due respect, the Office has read Applicants' invention into all the references. Furthermore, Applicants' claimed structure is straightforward, and should not pose any difficulty in understanding to a reasonable practitioner. This attorney is respectfully at a loss to understand the difficulty of the Office in making a proper review of Applicants' invention.

The rejections based on 35 U.S.C. §112 are respectfully traversed for the following reasons:

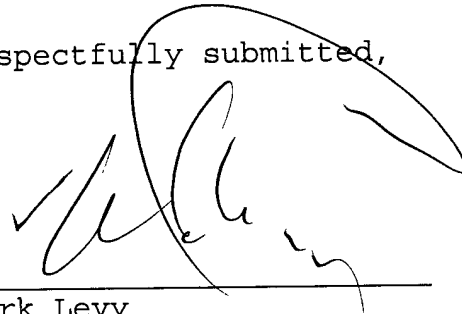
Applicant teaches electrically connecting vias of a signal core (single layer) to adjacent respective vias of an adjacent signal core (single layer) during a laminating process. This structure and method is straightforward, does

not require intricate claim drafting, and in fact has been claimed most succinctly. The questions and objections raised by the Office, with all due respect, make no sense.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "Version with markings to show changes made."

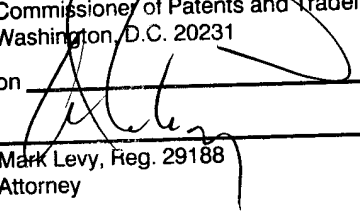
In view of the foregoing amendments and remarks, Applicants respectfully request that claims 1 through 7, and 11 through 14 be allowed and that the application be passed to issue.

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:



Claims 8 through 10 have been cancelled.

Claims 2 through 4, 6, and 7 have been amended as follows.

Claims 11 through 14 have been added.

2. (Amended) The multi-layered circuit structure in accordance with claim 1, wherein said first substrate comprises a signal core [layer], and said second substrate comprises a power core [layer].

3. (Amended) The multi-layered circuit structure in accordance with claim 1, wherein said first substrate comprises a pair of spaced-apart outer signal cores [core layers], and said second substrate comprises an inner power core [layer] sandwiched between said pair of spaced-apart outer signal cores [core layers].

4. (Amended) The multi-layered circuit structure in accordance with claim 3, wherein said via through holes of said inner power core [layer] comprise undercut contact surfaces, and said via through holes of said pair of spaced-apart signal cores [layer] have metallic pads that make electrical contact with said undercut contact surfaces of said via through holes of said inner power core [layer].

6. (Amended) The multi-layered circuit structure in accordance with claim 5, wherein said first substrate comprises a signal core [layer], and said second substrate comprises a power core [layer].

7. (Amended) The multi-layered circuit structure in accordance with claim 5, wherein said first substrate comprises a pair of spaced-apart outer signal cores [core layers], and said second substrate comprises an inner power core [layer] sandwiched between said pair of spaced-apart outer signal cores [core layers].

11. (Added) A multi-layered circuit structure, comprising:

first and second spaced-apart substrates, each having
conductive via through holes disposed therein; and

a third substrate laminated between said first and second
spaced-apart substrates and having conductive, adhesive-
filled via through holes that align with, and make
electrical contact with, the conductive via through holes
of said first and second spaced-apart substrates, upon
lamination of said first and second spaced-apart
substrates to said third substrate.

12. (Added) The multi-layered circuit structure in
accordance with claim 11, wherein said first and second
spaced-apart substrates comprise a signal core, and said third
substrate comprises a power core.

13. (Added) The multi-layered circuit structure in
accordance with claim 11, wherein said first substrate
comprises a pair of spaced-apart outer signal cores, and said
second substrate comprises an inner power core sandwiched
between said pair of outer signal cores.

14. (Added) The multi-layered circuit structure in accordance with claim 13, wherein said via through holes of said inner power core comprise undercut contact surfaces, and said via through holes of said spaced-apart outer signal cores each have metallic pads that make electrical contact with said undercut contact surfaces of said via through holes of said inner power core.